the absence of a valid signal from the second component, and in response to the valid signal from the second component, supplying the second clock signal to the buffer to clock data from the buffer to the second component via the data path without clocking other data from the first component to the buffer via the data path.

24. The apparatus of claim 23, wherein a ready signal from the first component is transmitted to the second component indicating that the transfer of data from the first component to the buffer is complete.

25. The apparatus of claim 23, wherein the buffer and multiplexer are part of an integrated circuit.

26. A method of transferring data between a first component and a second component in a computer system, the first component clocked by a first clock signal, and the second component clocked by a second clock signal, the first clock signal being out of sync with the second clock signal, comprising:

clocking data from the first component to a buffer via a data path using the first clock signal in the absence of a valid signal from the first component;

clocking data from the buffer to the second component via the data path using the second clock signal in response to the valid signal from the second component without clocking other data from the first component to the buffer via the data path; and

supplying the first and second clock signals to the buffer via a multiplexer having a plurality of inputs and an output coupled to the buffer, the inputs for receiving the first and second clock signals and a valid signal from the second component, the multiplexer supplying the second clock signal to the buffer in response to the valid signal.

27. The method of claim 26, further comprising transmitting a ready signal from the first component to the second component indicating that the transfer of data from the first component to the buffer is complete.

28. An apparatus for use in a computer system for transferring data between a plurality of components including at least one source component and at least one destination component, the source component clocked by a first clock signal, and the destination component clocked by a second clock signal, the first clock signal being out of sync with the second clock signal, comprising:

a buffer coupled to the source component and the destination component via a data path;

a multiplexer having inputs coupled to the first clock signal and the second clock signal, and an output coupled to the buffer, the multiplexer supplying the first clock signal to the buffer to clock data from the source component to the buffer via the data path in the absence of a gate signal from the destination component, the multiplexer supplying the second clock signal to the buffer to clock data from the buffer to the destination component via the data path in response to the gate signal from the destination component without clocking other data from the source component to the buffer via the data path; and

a broadcast bus coupled to the source component, the destination component and the buffer, the broadcast bus for transferring a ready signal from the source component to the destination component indicating that the transfer of data from the first component to the buffer is complete.

29. The apparatus of claim 28, wherein the source component places the address of the destination component on the broadcast bus and the destination component supplying the gate signal to the multiplexer in response to the address.

30. The apparatus of claim 28, wherein the buffer and the multiplexer are part of an integrated circuit.